REMARKS

Claims 1-21 are pending in the application, with claims 1-8 and 14-21 having been withdrawn from consideration.

Claim 12 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **January 15, 2003**.

Claim Rejections under 35 USC §112

Claim 12 has been amended, as needed, to overcome the rejection. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections under35 USC §103

Claims 9-13 are rejected under 35 USC §103(a) as being unpatentable over Applicant's admitted prior art in view of Wang (U.S. Patent No. 6,188,011 B1).

The present invention includes a buried bit line type semiconductor device, as a major precondition. In claim 9, it is clearly described that a gate electrode (word lines) is formed so as to cross source and drain regions (buried bit lines) over a semiconductor substrate with a multilayer film (ONO film) being interposed between them.

On the precondition of the above characteristics in construction, while the present invention requires ensuring electrical insulation between a gate electrode and source and drain regions, the present invention also requires suppressing undesirable bird's beak formation in advance. For

forming a lower film of the multilayer film having an appropriate thickness to balance both requirements, the source and drain regions are formed by introducing a substance having an accelerated oxidation suppressing function, such as nitrogen, as well as the impurities.

On the other hand, in Wang, as apparent from Figs. 1 to 4, a normal transistor structure is employed, in which source and drain are formed on both sidse of a gate electrode of a semiconductor substrate. Wang discloses an art for reducing diffusion of source and drain by introducing nitrogen after forming the gate electrode, in order to reduce short channel effect of Flash EPROM.

The present invention includes a main object of solving the characteristic problems pertinent to a construction and manufacturing method of a buried bit line type semiconductor device. Therefore, it is incompatible to combine APA of the present specification and the art for introducing nitrogen to suppress short channel effect in a normal transistor structure. The present invention and Wang are common only in that "nitrogen is introduced into source and drain", however, they are different 1) in specific constructions of a semiconductor device, 2) in the purpose of introducing nitrogen, and 3) in situations of manufacturing process of a semiconductor device.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "APA does not teach the source and drain containing a substance having anaccelerated oxidation suppressing function."

The Applicant agrees with this Office assessment of the shortcoming of the APA. However, to supplement this shortcoming, the outstanding Office Action further stated that:

> "Wang et al. teach a gate over a substrate between a source and drain region. Wang teach a substance in the source and drain that has an accelerated oxidation suppression function. Wang teach nitrogen dopants added to the source and drain region to reduce lateral diffusion of dopant material in the channel region and reduce short channel effects. APA and Wang are combinable because they are from the same

field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to dope the source and drain regions with nitrogen. The motivation for doing so is to reduce short channel effects and allow the device dimensions to be smaller. Therefore, it would have been obvious to combine APA with Wang to obtain the invention of claim 9."

There is a link as to the logics of combining these references, because the problems faced by APA and Wang are completely different. In the APA, as has already been clearly explained in the instant application, between page 6, last paragraph and page 8, line 7:

"In the manufacturing method described in the prior art 1, since electrical insulation between the bit lines 104 and the word lines 105 are ensured only by the ONO film 102, the breakdown voltage of the ONO film 102 must be made high. In this manufacturing method, however, since arsenic ions are ion-implanted through the ONO film 102 to form the bit lines 104, the ONO film 102 may be inevitably damaged. In addition, since the uppermost silicon oxide film 113 of the ONO film 102 may be partially or fully etched off through a post-process, it is hard to ensure a sufficient breakdown voltage of the ONO film 102.

In the manufacturing method described in the prior art 2, in thickening the silicon oxide film 111 above the bit lines 104 by annealing, only the silicon oxide film 111 is present above the bit lines 104. For this reason, bird's beaks may be formed on both sides of each channel region due to the wraparound by oxygen. In addition, since the peripheral circuit region is normally formed simultaneously with formation of the memory cell region, the silicon oxide film 111 above the bit lines 104 may become thicker (about 100 to 150 nm) through several times of annealing processes in forming the gate insulating films of transistors in the peripheral circuit region, and accordingly, larger bird's beaks may form.

In the manufacturing method described in the prior art 3, due to accelerated oxidation through each annealing process for the impurity diffusion to form the bit lines 104 and the formation of the ONO film 102, the sacrificial oxide film 106 above the bit lines 104 may increase its thickness, and large bird's beaks may also grow.

> As described above, in manufacturing a semiconductor memory having a buried bit line structure, it is difficult to ensure electrical insulation between the bit lines and the word lines, or even when electrical insulation can be ensured, it may cause bird's beak formation and considerably degrades the charge holding characteristic. These are serious problems."

Therefore, in prior art 1 of the APA, the technical problem is related to damages of the ONO film and difficulty of ensure a sufficient breakdown voltage. In prior art 2 of the APA, the technical problem is related to the formation of bird's peaks on both sides of the channel regions. In prior art 3 of the APA, the technical problem is related to formation of bird's peaks and ensuring electrical insulation between the bit lines and the word lines, and degradation of the charge holding characteristic.

In contradistinction thereto, Wang explains in column 1, from line 25-49 that:

> Presently, scaling down of Flash EPROM cells has been considered critical in continuing the trend toward higher device density. Typically, however, the scaling of cell size has not been accompanied by a scaling in the internal operation voltage requirement for the cell. As the size of the cells shrink, short channel effect becomes problematic. Short channel effect generally refers to the problem associated with drain induced barrier lowering (DIBL) and threshold voltage roll-off with channel length. With larger cell sizes, the channel between the source and drain is long and the transient electrical field generated is very small during the charging period, i.e., during the period when the voltage is applied to the source. However, as the channel becomes shorter due to cell size shrinkage, short channel effect becomes more problematic.
>
> Attempts to combat the problem of short channel effect include the reduction of doping in a source side implant. The reduction in doping usually leads to less diffusion of the source dopant in the channel. However, an inherent limit to the doping reduction exists, since a certain level of doping is required to maintain proper cell erase functionality.
>
> Accordingly, a need exists for a manner of reducing short channel effect in a Flash EPROM cell, while maintaining reliable cell operation through preferred doping levels."

Therefore, the technical problems of Wang is related to short channel effect due to miniturization of semiconductor devices. As the technical problems related to the APA and Wang are quite different, it is not understood why a person of ordinary skill in the art would in foresight, choose to combine them. To establish a *prima facie* case of obvious in foresight, section 2143 of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Therefore, it is both a court position and a Patent Office position that to establish a *prima facie* case of obviousness, 1) there **must be** some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there **must be** a reasonable expectation of success; and 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be** found in the prior art, and not based on applicant's disclosure.

In the combination rejection, the Applicants regretfully cannot find any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. The Applicants also cannot find the teaching or suggestion to make the claimed combination and the reasonable expectation of success in the prior art.

Therefore, it is respectfully submitted that claims 9-13 are not rendered obvious by the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

Should the Office finds other prior art references but is either unable to identified each and every aspect of the above-mentioned claimed features therein, or the formulated rejection simply would not arise to a level objectively fulfilling all three criteria of establishing a *prima facie* case of obviousness, it is respectfully submitted that the obviousness rejection would be defective and allowance of the claimed invention is requested.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicants' understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

Conclusion

In view of the aforementioned amendments and accompanying remarks, all pending claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Michael N. Lau
Attorney for Applicant
Reg. No. 39,479

MNL/eg
Atty. Docket No. **010999**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Drawing Replacement Sheets 1-3

H:\HOME\EGreenwood\MNL\01\010999 a3